Design of a Pulsed Hybrid Flip-Flop Using C-Element for Low Power Applications

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Submitted by

**2310040023: YASASWINI KOSURU**

**2310040059: BHANDARY HARIPRIYA**

**2310040070: PIREEKATLA PRIYANKA**

**2310049146: SAYYEDA KASHIFA KONAIN**

Under the guidance of

**Dr.Ngangbam Phalguni Singh**

**Dr.Vijay Rao Kumbhare**



Department of Electronics and Communication Engineering

Koneru Lakshmaiah Education Foundation, Aziz Nagar

Aziz Nagar – 500075

**CHAPTER 1**

**INTRODUCTION**

Modern electronic systems are no longer judged only by their speed or functionality—they are increasingly measured by how much energy they consume. From smartphones and laptops to Internet of Things (IoT) devices, today’s technology must deliver high performance while still being efficient enough to run on limited battery power. This growing demand for energy efficiency has made low-power design one of the most critical challenges in VLSI technology [1].

At the heart of these systems are **flip-flops (FFs)**, the basic storage elements that hold data and synchronize operations in digital circuits. Every register, every pipeline stage, and every sequential block relies on flip-flops. Unfortunately, they are also among the largest contributors to power consumption. This is because flip-flops are directly tied to the global clock, which itself accounts for **30–60% of the total power of a chip** [1], [2]. Each time the clock ticks, flip-flops switch—even when no useful work is being done—leading to wasted energy. Reducing the power wasted in these elements has therefore become a central focus for researchers and designers.

Conventional flip-flop designs, such as master–slave latches and dynamic flip-flops, have served digital systems well for decades. However, they are far from perfect. Master–slave flip-flops, for example, use more transistors and load the clock heavily, while dynamic latches suffer from glitches and higher power draw [3], [4]. To overcome these issues, newer designs like **dual-edge triggered flip-flops (DETFFs)** were introduced, which capture data on both rising and falling edges of the clock. While this helps reduce clock frequency, these designs often introduce additional switching activity and complexity [5].

A breakthrough in this area came with the concept of **pulsed flip-flops (P-FFs)**. Instead of keeping flip-flops sensitive throughout an entire clock cycle, P-FFs use a narrow pulse to capture data only when needed. This approach greatly reduces clock loading and improves energy efficiency [6]. Depending on how the pulse is generated, P-FFs are classified as **explicit** or **implicit**. Explicit types require external pulse generators, but they add more circuitry and power overhead. Implicit types embed the pulse logic inside the latch, but may struggle with timing and longer critical paths [6], [7]. Despite their limitations, pulsed flip-flops are widely regarded as more energy-friendly than traditional flip-flops, making them attractive for modern low-power designs [8].

As research progressed, several innovative P-FF architectures appeared, such as **semi-dynamic flip-flops (SDFF)** [4], **single-ended conditional capturing flip-flops (SCCER)** [8], and **dual dynamic node flip-flops (DDFF)** [5]. Each design tried to balance power, speed, and reliability, but trade-offs remained—some reduced power but consumed more area, while others improved delay but increased leakage power. This highlighted the need for a hybrid design that could deliver all three: low power, compact layout, and high performance.

One promising solution is to bring the **C-element** into flip-flop design. The C-element, widely used in asynchronous logic, changes its output only when all inputs match, holding its state otherwise. This simple mechanism helps prevent unnecessary switching and reduces wasted power. By combining the C-element with a pulsed flip-flop structure, researchers have achieved a clever hybrid that suppresses redundant activity while maintaining speed [1].

For instance, Rahiminejad and Saneei [1] proposed a **pulsed hybrid flip-flop using a C-element**, which showed remarkable results. Their design achieved **27.8% and 16.9% reductions in power consumption** at 25% and 50% data activity, respectively, compared to other well-known flip-flops. Even more impressive, it required only **17 transistors**, making it up to **12% smaller in layout area** than competing designs. This balance of power savings, compactness, and performance makes the hybrid C-element-based flip-flop an exciting candidate for next-generation VLSI systems.

In comparison with other designs such as SDFF [4], DDFF [5], and SCCER [8], the hybrid approach not only improves **power-delay-product (PDP)** but also offers better robustness against process variations and clock fluctuations [9]. This makes it particularly suitable for deep-submicron technologies, where variability and leakage are major concerns.

Given these advantages, our project focuses on exploring the design and simulation of a **pulsed hybrid flip-flop using a C-element**. By studying its structure, simulating it in Cadence Virtuoso, and comparing its performance against conventional designs, we aim to understand how this architecture can help build low-power, high-speed digital systems .

**PROBLEM STATEMENTS & OBJECTIVES**

**Problem Statement 1:**  
In modern VLSI systems, power efficiency has become a critical design constraint. Flip-flops, being clock-driven elements, switch at every clock edge and therefore contribute heavily to dynamic power consumption. Conventional designs often suffer from unnecessary switching, glitches, and high clock load, which makes them unsuitable for energy-constrained applications such as wearable devices, IoT nodes, and portable processors.

**Objective 1:**  
To design and analyze a **hybrid pulsed flip-flop incorporating a C-element**, with the aim of reducing redundant transitions and glitches, thereby minimizing overall dynamic power consumption.

**Problem Statement 2:**  
Traditional flip-flop architectures generally require a large number of transistors, leading to higher silicon area utilization and increased fabrication costs. When scaled to millions of instances in complex VLSI circuits, this results in larger chip area, reduced integration density, and inefficient hardware utilization.

**Objective 2:**  
To implement a **compact hybrid flip-flop design** that minimizes transistor count, thereby reducing silicon area and improving cost-effectiveness while maintaining performance.

**CHAPTER 2**

**METHODOLOGY**

The proposed project aims to design and analyze a **low-power pulsed hybrid flip-flop using a C-element** in **Cadence Virtuoso** with **90 nm CMOS technology**. The methodology is divided into five major phases: (1) literature review and problem identification, (2) schematic design, (3) layout design, (4) simulation and performance evaluation, and (5) comparative study with conventional flip-flops. This systematic approach ensures that the objectives of reduced power, minimized area, and improved robustness are met.

**1. Literature Review and Problem Identification**

The methodology begins with a comprehensive study of conventional flip-flop architectures to identify their strengths and weaknesses. Flip-flops such as **master–slave designs** and **semi-dynamic flip-flops (SDFFs)** have been widely used but are not efficient for modern low-power applications. Master–slave structures use more transistors and load the clock heavily, while SDFF suffers from glitches and high switching activity, leading to excessive power consumption [1], [2], [3], [4].

Other designs like **dual-edge triggered flip-flops (DETFFs)** and **dynamic explicit pulsed flip-flops (DEPFFs)** were proposed to improve performance. DETFFs reduce clock frequency but suffer from additional switching, while DEPFFs incur power overhead from the pulse generator [5], [6], [7]. Despite these limitations, **pulsed flip-flops (P-FFs)** remain attractive due to their reduced clock load and improved energy efficiency [6], [8].

Recent advancements introduced **C-element-based pulsed flip-flops**, which reduce redundant switching activity and improve the **power-delay product (PDP)**. Rahiminejad and Saneei [1] showed that integrating a C-element leads to significant power savings and area reduction. This motivates the design of a **hybrid pulsed flip-flop with a C-element**, which balances power, area, and performance, making it suitable for portable and IoT devices.

**2. Schematic Design in Cadence Virtuoso**

**2.1 Transistor-Level Design**

The hybrid pulsed flip-flop consists of three main stages:

* **Sampling Circuit:** Built using a small number of transistors to capture input data during the clock’s transparent window.
* **C-element Stage:** Ensures transitions only when both inputs match, thereby eliminating unnecessary switching [1].
* **Keeper Stage:** Maintains output stability during hold periods [1], [6].

The proposed design uses only **17 transistors**, compared to SDFF (23 transistors) and DEPFF (28 transistors) [4], [6]. This lower transistor count directly translates into reduced layout area and minimized power consumption.

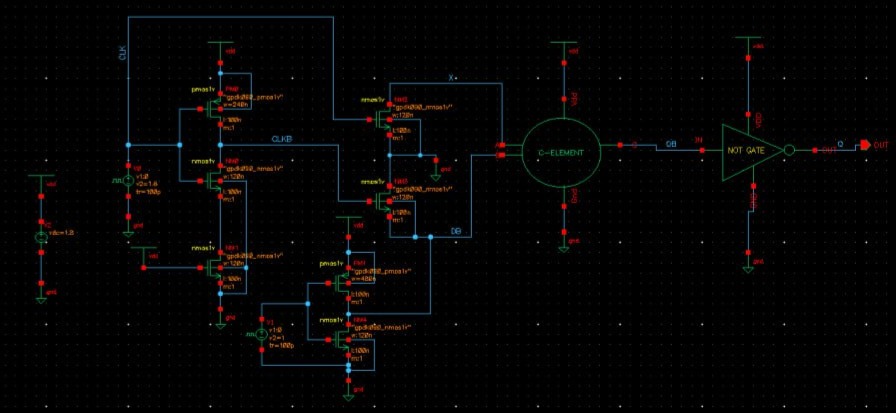


Fig.1.Proposed Design

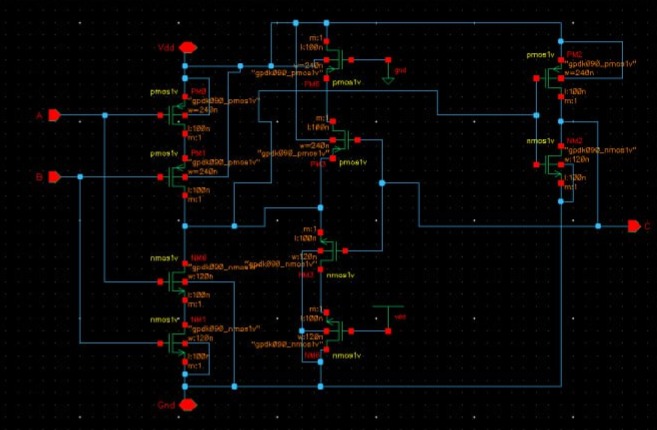


Fig.2.C-Element Schematic

**3. Layout Design**

After the schematic verification, the circuit is translated into a layout using **Virtuoso Layout Editor**. The key considerations in layout design include:

* **Transistor Sizing:** Optimized to balance speed and power.
* **Routing Strategy:** Careful placement and routing to minimize parasitic capacitances that can degrade performance.
* **Area Optimization:** Since the proposed design uses fewer transistors, its layout area is expected to be at least **12% smaller** than conventional flip-flops like DDFF and SCCER [5], [8].

Post-layout extraction is performed to evaluate the true performance by including parasitics, ensuring that the simulated results are realistic.

**4. Simulation and Performance Evaluation**

The design is simulated using **Cadence Spectre** across multiple test conditions.

**4.1 Performance Metrics**

The following parameters are measured to validate the design:

1. **Power Consumption:** Both dynamic and static power are measured for data activity factors of 0%, 25%, 50%, and 100%. The C-element is expected to reduce unnecessary transitions, leading to significant power savings [1], [6].
2. **Propagation Delay (D-to-Q Delay):** Measured as the minimum time for data to propagate to the output after a clock edge [7].
3. **Power-Delay Product (PDP):** Provides a combined measure of speed and power efficiency. Previous research reported PDP improvements of **up to 55.7%** for C-element-based designs [1].
4. **Setup and Hold Time:** Setup time is the minimum time before the clock edge for stable data, while hold time is the stability required after the clock edge. These are crucial for reliability in sequential circuits [7], [9].
5. **Area Efficiency:** Extracted from the layout and compared with conventional designs. The proposed design, with only 17 transistors, is expected to be more area-efficient [1].

**5. Comparative Study**

Finally, the proposed flip-flop is compared with existing designs, including:

* **Semi-dynamic flip-flop (SDFF)** [4]
* **High-speed dual-edge modified hybrid latch flip-flop (HSDMHLFF)** [5]
* **Dynamic explicit pulsed flip-flop (DEPFF)** [6]
* **Single-ended conditional capturing flip-flop (SCCER)** [8]
* **Dual dynamic node flip-flop (DDFF)** [5]

The comparison is based on **power consumption, delay, PDP, layout area, and robustness**. Results are presented in both tabular and graphical form to clearly highlight the improvements.

By following this methodology, the project aims to validate the effectiveness of the **C-element based pulsed hybrid flip-flop** in achieving **low power, compact area, and high performanc**

**CHAPTER 3**

**LITERATURE SURVEY**

**1. Introduction to Flip-Flops in VLSI Systems**

Flip-flops are fundamental sequential elements in digital systems, used for data storage, synchronization, and pipeline control. Every modern processor, memory unit, and digital controller relies on millions of flip-flops to function correctly. However, with the continuous scaling of CMOS technologies, flip-flops have emerged as a **major source of power consumption and area overhead** in VLSI systems [1].

Since flip-flops are clock-driven, they switch every clock cycle, regardless of whether the input data changes or not. This results in significant **dynamic power consumption**, as the global clock itself consumes nearly **30–60% of total chip power** [1], [2]. In addition, timing issues such as setup and hold violations, combined with higher transistor counts in conventional designs, make flip-flops a bottleneck in modern low-power VLSI systems.

This section provides a comprehensive review of flip-flop designs, from conventional master–slave and dynamic structures to modern low-power approaches such as pulsed flip-flops (P-FFs), dual-edge triggered flip-flops (DETFFs), and C-element-based hybrids.

**2. Conventional Flip-Flop Architectures**

**2.1 Master–Slave Flip-Flops**

The master–slave flip-flop is the most widely taught and historically significant sequential element. It consists of two latches connected in series: the master latch captures data on one clock phase, and the slave latch updates the output on the opposite phase. While robust and easy to design, this architecture suffers from **high transistor count** and **large clock loading**, which translate into higher area and dynamic power consumption [1], [3].

**2.2 Dynamic Flip-Flops**

Dynamic flip-flops were introduced to improve performance by reducing the number of switching transistors during operation. However, these designs are prone to **glitches**, **charge leakage**, and timing uncertainty, making them less reliable in deep-submicron technologies [4]. Furthermore, dynamic structures consume significant power due to spurious switching, which limits their use in low-power applications.

**3. Semi-Dynamic and Hybrid Designs**

To overcome the drawbacks of purely static and purely dynamic designs, researchers introduced **semi-dynamic flip-flops (SDFFs)** [4]. These combine static storage with dynamic capturing to improve speed. While SDFFs achieve high performance, they still suffer from excessive power consumption due to unnecessary switching activity, especially in high-frequency designs [4].

Hirata *et al.* [3] later proposed the **cross-charge control flip-flop**, a design suitable for mobile SoCs that balances speed and power. While it improved delay, its complexity and transistor overhead limited scalability in deep-submicron systems. These studies highlight the ongoing trade-off between **speed, power, and area** in flip-flop design.

**4. Dual-Edge Triggered Flip-Flops (DETFFs)**

One approach to reducing power is to capture data on both rising and falling edges of the clock, effectively halving the clock frequency. This is the principle behind **dual-edge triggered flip-flops (DETFFs)**. Tschanz *et al.* [2] showed that DETFFs can improve performance for high-speed microprocessors, but they often suffer from **increased switching activity** and **design complexity**, limiting their overall energy efficiency.

Similarly, later modifications such as the **High-Speed Dual-Edge Modified Hybrid Latch Flip-Flop (HSDMHLFF)** improved delay performance but required more transistors, leading to larger silicon area [5]. Thus, DETFF-based designs reduce clock power but often increase local flip-flop complexity, resulting in mixed results for overall chip efficiency.

**5. Pulsed Flip-Flops (P-FFs)**

**5.1 Explicit vs. Implicit Pulsed Designs**

Pulsed flip-flops emerged as a promising alternative by using **short clock pulses** instead of the full clock cycle. This greatly reduces clock load and improves energy efficiency [6].

* **Explicit P-FFs:** Generate pulses using external circuits. While they achieve high performance, they require additional pulse generators, which increase transistor count and power overhead [6].
* **Implicit P-FFs:** Integrate pulse generation within the latch itself, making the design more compact. However, they often face timing challenges due to longer critical paths [6], [7].

Despite these drawbacks, pulsed flip-flops are widely regarded as **more power-efficient** than conventional flip-flops, especially for low-power VLSI systems [8].

**5.2 Advanced P-FF Variants**

Several researchers have proposed enhancements to the P-FF concept:

* **Single-Ended Conditional Capturing Flip-Flops (SCCER):** Reduce unnecessary switching by conditionally capturing transitions, improving energy efficiency [8].
* **Dual Dynamic Node Flip-Flops (DDFF):** Reduce delay but suffer from area overhead due to additional transistors [5].
* **Conditional Pulse Enhancement Schemes:** Proposed by Hwang *et al.* [6], which improved the robustness of P-FFs under process variations while maintaining low power.

These studies show that while P-FFs are attractive, most variants still struggle with either **area efficiency** or **robustness**, leaving room for improvement.

**6. Low-Power Clocking Techniques**

Beyond flip-flop structures, reducing power in the **clock distribution network** is equally important. Mahmoodi *et al.* [8] proposed ultra-low-power clocking schemes using **energy recovery and clock gating**, which reduced overall dynamic power significantly. Zhao *et al.* [9] further explored sequential elements optimized for low-power clocking, showing that careful integration of clock and flip-flop design can achieve better system-wide energy efficiency.

These works highlight that both **local flip-flop design** and **global clocking strategies** must be optimized together to achieve true low-power operation.

**7. C-Element-Based Hybrid Flip-Flops**

The **C-element**, traditionally used in asynchronous logic, outputs a signal only when all inputs agree, otherwise holding its previous state. This makes it effective at suppressing redundant switching activity. Rahiminejad and Saneei [1] integrated the C-element into a **hybrid pulsed flip-flop** design, demonstrating significant improvements.

Key results included:

* **27.8% power reduction at 25% activity**, and **16.9% at 50% activity**, compared to conventional designs [1].
* **12% area savings** with only 17 transistors [1].
* Improved **power-delay-product (PDP)** and robustness against process variations [1].

This work shows that the C-element-based hybrid flip-flop strikes a better balance between **power, area, and speed**, making it highly suitable for next-generation ASIC and FPGA applications.

A diagram of a circuit

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Fig.3.C-element based pulsed hybrid flipflop,(a).Circuit Diagram,(b)Timing Diagram

**8. Comparative Insights**

A review of literature across multiple designs reveals the following:

* **Conventional Flip-Flops (Master–Slave, Dynamic, SDFF):** Reliable but suffer from high transistor count, power, and glitches [3], [4].
* **DETFFs and HSDMHLFFs:** Reduce clock frequency but often introduce additional switching power [2], [5].
* **Pulsed Flip-Flops (Explicit/Implicit):** Reduce clock load but face challenges of pulse generation overhead or timing degradation [6], [7].
* **Advanced Variants (SCCER, DDFF):** Improve performance but at the cost of area or robustness [5], [8].
* **C-Element Hybrids:** Achieve significant improvements in power and area while maintaining robustness, addressing most limitations of earlier designs [1], [9].

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